REMARKS

Claims 2-4, 6, 7, 9, 10, 11, 13-16 are pending in this application. Claims 2, 3, 6, 7, 9, 10, 13, and 14 are independent. Claims 1, 5, 8, and 12 have been canceled.

Claim Rejection – 35 USC 103; Brown and Fehr

Claims 1-16 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al. (U.S. Patent 5,267,842) and Fehr (U.S. Patent 6,058,602). NOTE: The rejection incorrectly states the rejection as being under 35 U.S.C. 102(b). For the sake of argument, it will be assumed that the rejection was intended to be under 35 U.S.C. 103(a). Applicants respectfully traverse this rejection.

Claims 1, 5, 8, and 12 have been canceled. Claims 2 and 9 have been re-written into independent form. Claim 15 now depends from claim 2.

At the outset, a major difference between Brown and the present invention is that Brown is concerned with a controller and associated protocol for system wide testing of a multiplicity of printed circuit boards, each board having a standard ring connection of chips (e.g., Brown's prior art Figure 2), whereas the present invention is directed to various specific designs and arrangements of the chips to accommodate the standard testing protocol (present Figures 1-5). Brown deals with extending the IEEE Std 1149.1 to a system of circuit boards. The present invention deals with improving the design of a package of chips within the

IEEE standard. Thus, Brown and the present invention are directed to alternative approaches for dealing with testing based on the IEEE Std 1149.1.

Claim 2 (see **Figures 3 and 4**) is directed to a semiconductor device comprising a plurality of chips, which are integrally sealed air-tight (e.g., see Figures 2 and 4); a test signal input terminal (e.g., Figures 1 and 3, pin BI); a test result output terminal for outputting a test result of the plurality of chips to outside (e.g., Figures 1 and 3, pin B0); and control signal input terminals (e.g., Figures 1 and 3, pins BC, BM, and BR), the test signal inputted from the test signal input terminal being successively transferred through the plurality of chips (e.g., Figure 3, wire W0 and W0I connecting signal line TDO to TDI), and the test control signals inputted from the control signal input terminals being individually supplied to each of the plurality of chips (e.g., Figure 3, signal lines TCK, TMS, TRST connected, parallel to each other, via wires WC, WM, and WR). Further, claim 2 is directed to a plurality of chips connected to each other via the test result output terminal (Figure 4, where chips in a dual in line (DIL) structure, being mounted on front and back surfaces of a substrate 32, are connected to each other via test commands/data output pin B0; specification at paragraph bridging pages 17 and 18).

The Office Action alleges that Brown and Fehr teach the limitations of former claim 1 and that Brown teaches the claimed plurality of chips connected to each other through test output terminal, at column 4, lines 3-27. Fehr is relied on

for teaching that IC chips are typically packaged in an air-tight environment, at column 1, lines 35-40.

Applicants submit that Brown fails to teach or suggest the claimed, "wherein said plurality of chips are connected to each other via said test result output terminal." As can be seen in Brown, TDO designates the test data output pin (Brown, column 3, line 64). A standard-compliant board has leads including TDO (Brown, column 4, lines 3-6). The TDO pin of a first chip is connected to the TDI pin of the second chip, the TDO pin of the second chip is connected to the TDI pin of the third chip, and the TDO of the last chip goes to the external test bus' TDO line (Brown, column 4, lines 12-16). Thus, unlike Brown, the present invention is directed to a plurality of chips connected to each other via the test result output terminal. Applicants submit that Fehr fails to make up for this deficiency in Brown.

Furthermore, Brown's Figure 2 merely discloses a plurality of chips mounted on a circuit board (i.e., standard-compliant board having a single ring of daisy-chained chips; as described in Brown: column 4, lines 16-27). Despite allegations in the Office Action, Brown is completely silent with respect to disclosure of air-tight sealed packaging. Fehr specifically refers to IC's individually packaged, and explicitly states that, "In an IC packaging molding operation, <u>individual dies are encapsulated</u> in a plastic-polymer material, <u>leaving conductive leads protruding</u> from the finished plastic package" (Fehr: column 2, lines 2-5). Fehr, also, is completely silent with respect to disclosure of a plurality of chips

integrally sealed air-tight. These same arguments apply as well to claim 9. Thus, for at least these reasons the rejection fails to establish *prima facie* obviousness for claims 2 and 9.

Claim 3 (see **Figures 4 and 5**) is directed to a semiconductor device comprising a plurality of chips, which are integrally sealed air-tight (e.g., Figure 4); a test signal input terminal (e.g., pin BI); a test result output terminal (e.g., pin B0); control signal input terminals (e.g., pins BC, BM, and BR), only one of the plurality of chips being connected to the test signal input terminal, to the test result output terminal, and to the control signal input terminals (e.g. Figure 5, where the one chip ic1a is connected to wires WI, W0, WC, WM, and WR; specification, page 20, lines 19-23), the test signal being inputted to the one of said plurality of chips and successively transferred through the other chips, and after being inputted again into the one of said plurality of chips, outputted as the test result outside (e.g., Figure 5, connections via wires W0I and W0), the test control signals being individually supplied from the one of the plurality of chips to each of the other chips (e.g., Figure 5, connections via wires W10, W11, W12).

The Office Action alleges that although Brown admittedly does not explicitly teach a single chip connected to the test signal input terminal and test result output terminal whereby the test signal is transferred to the other chips, "Brown et al. teach mechanics of testing and capable of transferring data between on-chip logic side and the pin by which the chip is connected to the rest of the system (other chips) (see col. 4, lines 28-45)." That section discloses possible data transfer

between cells, depending on control signals applied to that cell. Brown only discloses a single basic daisy-chained arrangement of chips on a circuit board (Figure 2) as Brown is directed to an apparatus and protocol for multi-drop application of IEEE Std 1149.1 to each board coupled in parallel to a system level controller through a master test bus (see "Field of the Invention"). In other words, Brown is concerned with a controller and associated protocol for testing a standard ring of devices.

However, Applicants submit that unlike Brown, the semiconductor device of claim 3 is directed to a structure where "only one of said plurality of chips being connected to said test signal input terminal, to said test result output terminal, and to said control signal input terminals." This same difference applies as well to claim 10.

Thus, for at least these reasons the rejection fails to establish *prima facie* obviousness for claims 3 and 10.

Claim 6 (see **Figures 3, 4, and 6**) is directed to a semiconductor device in which a plurality of chips are integrally sealed air-tight (e.g., Figure 4) comprising a test register provided between a core logic and each of input and output terminals of each chip (e.g., Figure 6, boundary scan register 2); and a control circuit for controlling the test register (e.g., TAPC 7), a test commands/data input terminal of a device (e.g., Figure 3, TDI of device 31) being connected to the test commands/data input terminal of a chip of a first stage (e.g., Figure 3, TDI of ic1), and the test commands/data output terminal of a chip (e.g., Figure 3, TDO of ic1)

being connected to a corresponding output terminal of the device (e.g., Figure 3, TDO of device 31) and serially to the test commands/data input terminal of a chip of a following stage via the output terminal of the device (e.g., Figure 3, TDI of ic2 via wire W0I), and input terminals of the device for the signals to be used in the test (e.g., Figure 3, TCK, TMS, and TRST via wires WC, WM, and WR) being connected to the corresponding input terminals of the signals of each chip.

Applicants agree with the Office Action which states that Brown teaches circuit boards loaded with standard – compliant devices/chips connected together into test rings by local test buses accessible at the edge connectors. The Office Action directs Applicants' attention to Figure 2 of Brown for teaching the structural arrangement recited in claim 6. Applicants disagree that Figure 2 of Brown teaches the structural arrangement recited in claim 6.

As can be seen in Brown's Figure 2, edge connector TDI is connected to the corresponding input pin in a first chip in the ring. Because of the ring arrangement in Brown, the output pin of the first chip is connected to the input pin of the second chip in the ring (as an indication of which pin of the TAP is the test output pin, note the fourth chip and its pin connecting to the edge connector TDO). The output pin of the fourth chip is connected to the output edge connector TDO. Unlike Brown, the claimed invention has a test commands/data output terminal of a chip being connected to a corresponding output terminal of the device and serially to the test commands/data input terminal of a chip of a

following stage via the output terminal of the device. A similar argument can be made for claim 13.

Thus, at least for this reason, Applicants submit that the rejection fails to establish *prima facie* obviousness for claims 6 and 13.

Claim 7 (see **Figures 4, 5, and 6**) is directed to a semiconductor device in which a plurality of chips are integrally sealed air-tight comprising a test register provided between a core logic and each of input and output terminals of each chip (e.g., Figure 6, boundary scan register 2); and a control circuit for controlling the test register for the chip (e.g., TAPC 7), test commands/data input and output terminals of a device (e.g., Figure 5, TDI and TDO of the device 41) being respectively connected to the test commands/data input and output terminals of the chip of the first stage (e.g., Figure 5, TDI and TD0a of ic1a, respectively), and the relay output terminal of the chip of the first stage (e.g., Figure 5, TDO of ic1a) being connected to a test commands/data input terminal of a chip of a following stage (e.g., Figure 5, TDI of ic2a), and a test commands/data output terminal (e.g., Figure 5, TDO of ic2a) and a test commands/data input terminal (e.g., Figure 5, TDI of ic3a) being serially and successively connected between chips of a preceding stage and a following stage, and a test commands/data output terminal of a chip of a last stage (e.g., Figure 5, TDO of ic3a) being connected to the relay input terminal of the chip of the first stage (e.g., Figure 5, TDIa of ic1a) so as to form a loop, and the output terminals of the chip of the first stage for the signals to be used in the test (e.g., Figure 5, TAP0 to TAP4 of ic1a) being connected to

input terminals of the signals of the other chips (e.g., Figure 5, TAP0 to TAP4 of ic2a and 1c3a, respectively).

The Office Action alleges that although Brown admittedly does not explicitly teach a single chip connected to the test signal input terminal and test result output terminal whereby the test signal is transferred to the other chips, "Brown et al. teach mechanics of testing and capable of transferring data between on-chip logic side and the pin by which the chip is connected to the rest of the system (including other chips) (see col. 4, lines 28-45)." That section discloses possible data transfer between cells, depending on control signals applied to that cell. Brown only discloses a single basic daisy-chained arrangement of chips on a circuit board (Figure 2) as Brown is directed to an apparatus and protocol for multi-drop application of IEEE Std 1149.1 to each board coupled in parallel to a system level controller through a master test bus (see "Field of the Invention"). In other words, Brown is concerned with a controller and associated protocol for testing a standard ring of devices.

In Brown's Figure 2, the edge connection input terminal TDI is connected to the first chip and the edge connection output terminal TD0 is connected to the fourth/last chip. The output pin of the first chip is connected to the input pin of the second chip, and continues in this manner around the ring of chips to the last chip. In the present invention of claim 5, on the other hand, the test output terminal of the semiconductor device is connected to the test output terminal of the chip of the first stage, the relay output terminal of the chip of the first stage is

connected to a test input terminal of a chip of a following stage, as well as, a test output terminal of a chip of a last stage is connected to the relay input terminal of the chip of the first stage so as to form a loop. Applicants submit that Brown fails to teach this claimed structure. A similar argument can be made for claim 14.

Thus, at least for this reason, Applicants submit that the rejection fails to establish *prima facie* obviousness for claims 7 and 14.

In addition, with respect to claims 15 and 16 (see **Figure 4**), Brown and Fehr, either alone or in combination, fail to teach or suggest wherein the plurality of chips are stacked. Accordingly, Applicants submit that for at least this additional reason, the rejection fails to establish *prima facie* obviousness for claims 15 and 16.

Accordingly, Applicants respectfully request that the rejection be withdrawn.

CONCLUSION

Should the Examiner have any questions concerning this application, the Examiner is invited to contact Robert W. Downs (Reg. No. 48,222) at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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